

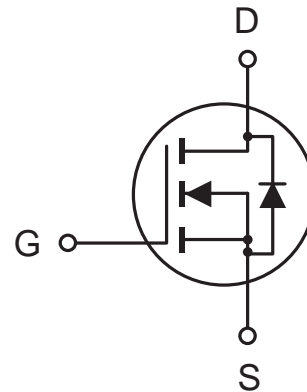
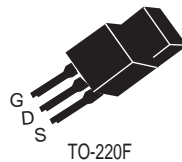
# CEF10N4

Sep. 2002

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### FEATURES

- 450V ,5.6A , $R_{DS(ON)}=700m\Omega$  @ $V_{GS}=10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- TO-220F full-pak for through hole.



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### ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	450	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous -Pulsed	$I_D$	5.6	A
	$I_{DM}$	17	A
Drain-Source Diode Forward Current	$I_S$	5.6	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	45	W
		0.36	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.8	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	65	$^\circ\text{C/W}$

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## ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE AVALANCHE RATING<sup>a</sup></b>						
Single Pulse Drain-Source Avalanche Energy	E <sub>AS</sub>	V <sub>DD</sub> = 50V, L = 9.16mH R <sub>G</sub> = 25 Ω		450		mJ
Maximum Drain-Source Avalanche Current	I <sub>AS</sub>			10		A
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	450			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 450V, V <sub>GS</sub> = 0V		25	100	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V		±100	±500	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2		4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		600	700	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 10V	10			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> = 6A	3	6		S
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> = 200V, I <sub>D</sub> = 10A, V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 9.1Ω		14	75	ns
Rise Time	t <sub>r</sub>			27	125	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			50	100	ns
Fall Time	t <sub>f</sub>			24	60	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 320V, I <sub>D</sub> = 10A, V <sub>GS</sub> = 10V		48	65	nC
Gate-Source Charge	Q <sub>gs</sub>			4	7	nC
Gate-Drain Charge	Q <sub>gd</sub>			15	25	nC

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$		1400		pF
Output Capacitance	$C_{OSS}$			330		pF
Reverse Transfer Capacitance	$C_{RSS}$			120		pF
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0\text{V}, I_S=10\text{A}$			2.0	V

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### Notes

a. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

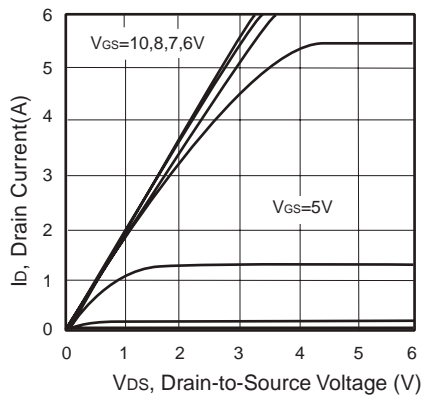


Figure 1. Output Characteristics

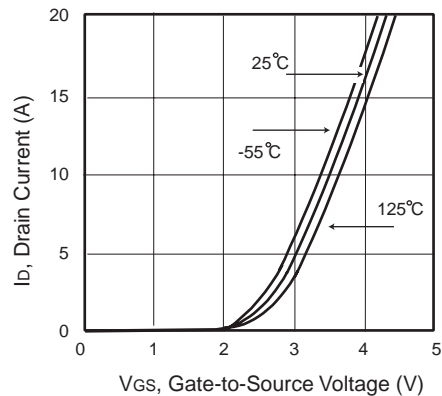
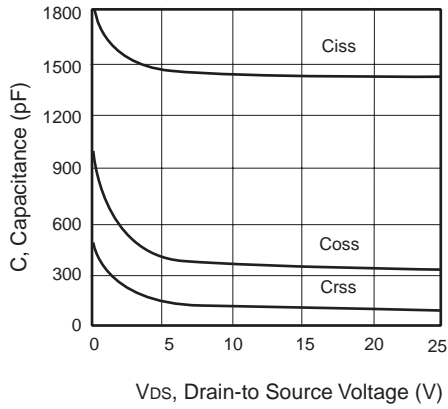


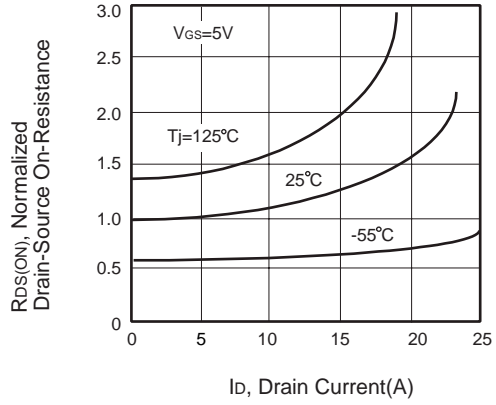
Figure 2. Transfer Characteristics

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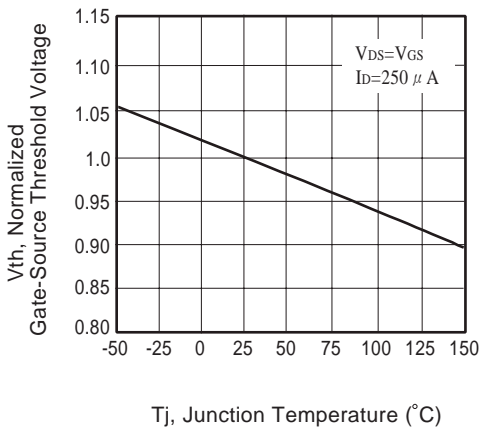
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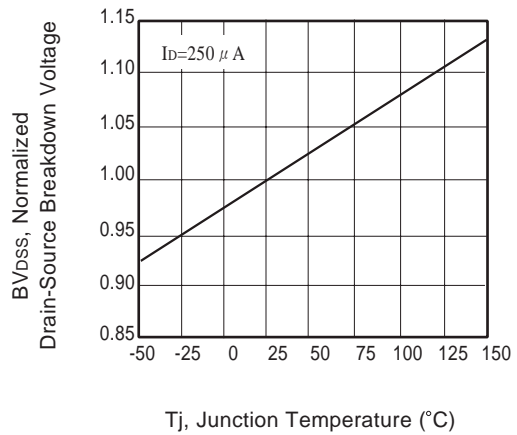
**Figure 3. Capacitance**



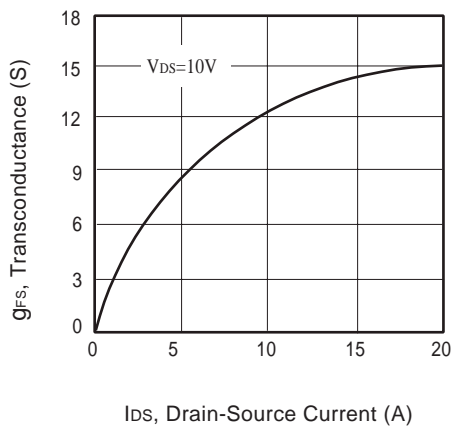
**Figure 4. On-Resistance Variation with Drain Current and Temperature**



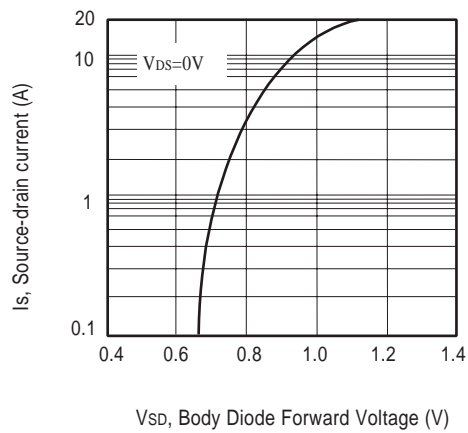
**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Breakdown Voltage Variation with Temperature**



**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**

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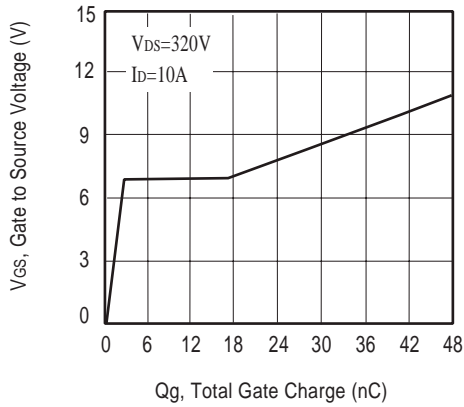


Figure 9. Gate Charge

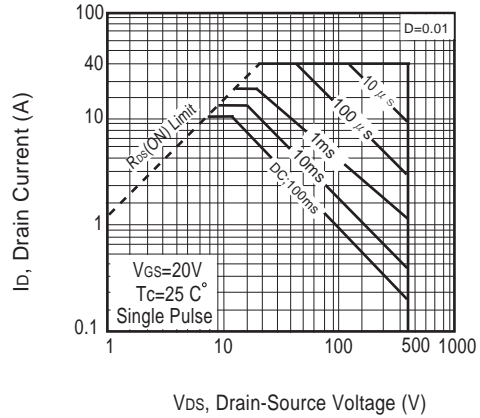


Figure 10. Maximum Safe Operating Area

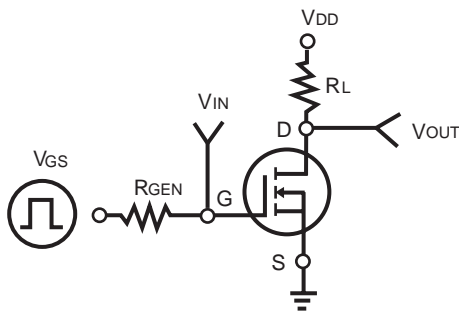


Figure 11. Switching Test Circuit

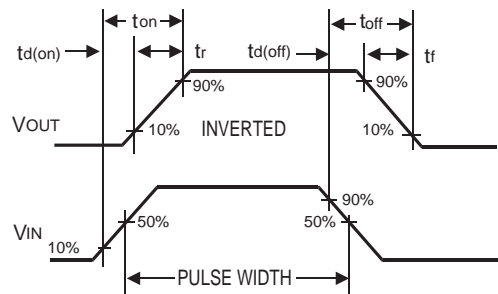


Figure 12. Switching Waveforms

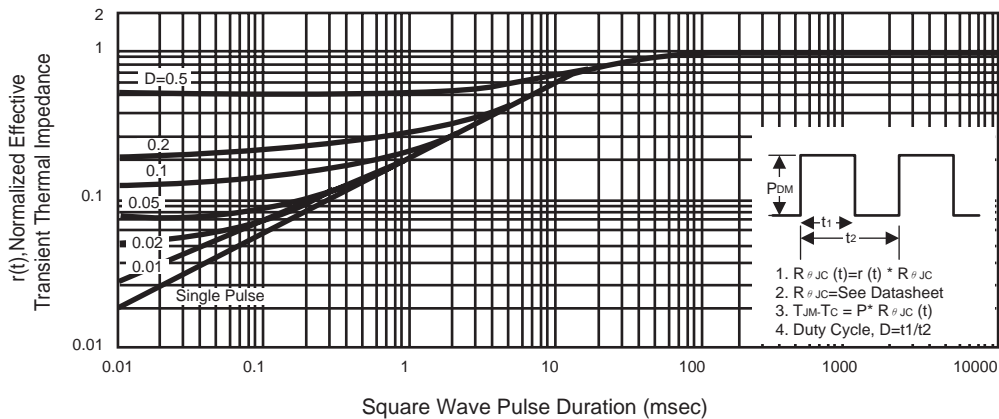


Figure 13. Normalized Thermal Transient Impedance Curve